

What Is Claimed Is:

1. A power semiconductor device having high avalanche capability, said device comprising:
an N⁺ doped substrate and, in sequence, N⁻ doped, P⁻ doped, and P⁺ doped semiconductor layers, said P⁻ doped and P⁺ doped layers having a combined thickness of about 5 μm to about 12 μm; and
recombination centers comprising noble metal impurities disposed substantially in said N⁻ doped and P⁻ doped layers.
2. The device of claim 1 wherein said P⁻ doped layer has a thickness of about 4 μm to about 10 μm.
3. The device of claim 1 wherein said P⁺ doped layer has a thickness of about 0.1 μm to about 2 μm.
4. The device of claim 1 wherein said P⁻ doped layer has a dopant level of at least 10¹⁶ atoms/cm³.
5. The device of claim 4 wherein said P⁻ doped layer has a dopant level of about 2.5x 10¹⁷ atoms/cm³.
6. The device of claim 1 wherein said P⁺ doped layer has a dopant level of at least 10¹⁸ atoms/cm³.
7. The device of claim 6 wherein said P⁺ doped layer has a dopant level of about 6x10¹⁹ atoms/cm³.
8. The device of claim 1 wherein said N⁻ doped layer has a dopant level of about 10¹⁴ atoms/cm³ to about 10¹⁵ atoms/cm³

9. The device of claim 1 wherein said N⁻ doped, P⁻ doped, and P⁺ doped semiconductor layers are epitaxial layers.

10. The device of claim 1 wherein said noble metal impurities are selected from the group consisting of gold, platinum, and palladium.

11. The device of claim 10 wherein said noble metal impurities comprise platinum.

12. The device of claim 11 wherein said recombination centers are formed by platinum diffusion through said N⁺ doped substrate into said N⁻ doped and P⁻ doped layers.

13. The device of claim 11 containing platinum impurities at a concentration of about 1×10^{15} to about 1×10^{16} atoms/cm³.

14. The device of claim 13 wherein said concentration of platinum impurities is about 2×10^{15} atoms/cm³.

15. The device of claim 1 further comprising an N⁺ doped region disposed in said N⁻ doped layer.

16. The device of claim 1 further comprising an N⁺ doped region disposed adjacent said P⁺ and P⁻ doped layers.

17. The device of claim 16 comprising a MOSFET or an IGBT power device.

18. A process for forming a power semiconductor device having high avalanche capability, said process comprising:

forming an N⁻ doped epitaxial layer on an N⁺ doped substrate;

forming a P⁻ doped layer in said N⁻ doped epitaxial layer;

forming a P⁺ doped layer in said P⁻ doped layer, said P⁺ doped and P⁻

doped layers having a combined thickness of about 5 μ m to about 12 μ m; and
forming in said P⁻ doped and N⁻ doped layers recombination centers
comprising noble metal impurities.

19. The process of claim 18 wherein said P⁻ doped layer has a thickness of
about 4 μ m to about 10 μ m.

20. The process of claim 18 wherein said P⁺ doped layer has a thickness of
about 0.1 μ m to about 2 μ m.

21. The process of claim 18 wherein said P⁻ doped layer has a dopant level of at
least 10¹⁶ atoms/cm³.

22. The process of claim 21 wherein said P⁻ doped layer has a dopant level of
about 2.5x 10¹⁷ atoms/cm³.

23. The process of claim 18 wherein said P⁺ doped layer has a dopant level of at
least 10¹⁸ atoms/cm³.

24. The process of claim 23 wherein said P⁺ doped layer has a dopant level of
about 6x10¹⁹ atoms/cm³.

25. The process of claim 18 wherein said N⁻ doped layer has a dopant level of
about 10¹⁴ atoms/cm³ to about 10¹⁵ atoms/cm³

26. The process of claim 18 wherein said noble metal impurities are selected from
the group consisting of gold, platinum, and palladium.

27. The process of claim 26 wherein said noble metal impurities comprise
platinum.

